Ohmic Contacts to Semiconducting Diamond

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Abstract—Natural semiconducting diamond samples (Class II-b) were used to develop techniques for the production of reproducible low-resistivity ohmic contacts for diamond devices. Annealed tantalum/gold and titanium/gold deposits on [100] polished diamond surfaces reduced the resistance by seven orders of magnitude relative to the as-received samples. The interfaces were characterized using metallography, scanning electron microscopy, and secondary ion mass spectrometry.

I. INTRODUCTION

SEMICONDUCTING diamond exhibits a unique combination of electrical, optical, and physical properties, e.g., low thermal impedance, low dielectric constant, high strength, excellent corrosion resistance, high breakdown voltage, radiation hardness, high saturated carrier velocities at high electric fields, and optical transparency over a wide frequency range.

The growth of boron-doped diamond films, by plasma-assisted CVD, with an electrical resistivity in the range of 0.001–1 Ω·cm was reported to be monocrystalline when deposited on a diamond substrate and polycrystalline when deposited on a silicon substrate [1]. More recently, the first diamond transistor with power gain has been reported [2]. Electrical contacts to these devices were obtained using tungsten point contacts.

Metal contacts applied to the smooth surfaces of semiconducting diamonds have exhibited extremely large electrical impedance due to the large potential barrier of approximately 4 eV [3]. Although a variety of techniques have been used to obtain electrical contacts to natural and synthetic diamonds [3], [4], these techniques have not yet been evaluated to determine the most desirable approach for device fabrication. This letter reports on a solid-state reaction process for producing ohmic contacts to polished natural semiconducting diamond surfaces. The approach attempts to systematically characterize the processes which occur when metallic films of known thickness are deposited on a smooth diamond surface and annealed in the solid state under controlled conditions.

II. RESULTS

The natural semiconducting diamond samples (Class II-b) used in this study were square plates with edge dimensions of 5 mm and a thickness of 0.25 mm. The crystallographic orientation of the faces was {100} and of the edges {110}. The current-potential (I–V) characteristics of the samples were measured using a pair of sharp tungsten probes with a separation distance of ~0.5 mm. An applied potential of 10-V dc produced a current of less than 0.1 pA. The electrical response of the as-received samples to higher ac applied potentials, prior to reaching the "threshold" potential, was typified by the behavior which is illustrated in Fig. 1. The "threshold" potential varied from sample to sample in the range of 300–1000 V. Once the "threshold" potential was reached, a current of ~10⁻⁵ A flowed at potentials substantially less than the "threshold" potential. The response of a sample after a "threshold" potential of 350-V ac was applied to it is seen in Fig. 2, where a current of ~2 × 10⁻⁷ A flows at a potential of 150-V ac.

Each corner of a 5 × 5-mm² face of a diamond sample was metallized sequentially with titanium and with gold and annealed to produce ohmic contacts, using procedures which will be described later. Wire leads were attached to the metallized corners for Hall effect measurements. The Hall mobility, carrier concentration, and resistivity measurements were made over the temperature range of 170–380 K using the Van der Pauw technique. The carrier concentration varied from 3 × 10¹⁴ cm⁻³ at 380 K to 3 × 10¹² cm⁻³ at 170 K, while the resistivity varied from 9 × 10³ to 2 × 10⁶ Ω·cm in the same temperature interval. The carrier activation energy was 0.32 eV in the interval of 277 to 380 K, in agreement with published results for natural diamond [1].

Using photolithography and a Shokley pattern mask, a grid of metallic pads of known area and of known variable spacings was deposited on the diamond ((C)) surface. A gold (Au) film, 150 nm thick, was sequentially deposited on top of a tantalum (Ta) film, 10 nm thick, in an ion-pumped ultra-high vacuum system using an electron-beam evaporation source. After the removal of the resist, a nonohmic current of ~1 pA at a potential of 10-V dc was measured.

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Next, the (C)/Ta/Au sample was annealed for 1 h at 885°C in a quartz tube furnace in an atmosphere of flowing purified hydrogen gas. The annealed sample exhibited linear dependence of current to the applied potential (illustrated in Fig. 3). The annealing process had reduced the resistance from a value of $\sim 10 \, \Omega$ to a value of 3.5 k$\Omega$, a reduction of approximately seven orders of magnitude.

Metallographic examination of the annealed sample revealed a significant reduction in the thickness of the gold deposit, by evaporation, during the annealing cycle. To prevent the possibility of short circuiting between pads by evaporation and recondensation during annealing, all subsequent samples were capped by a silicon nitride film (200–300 nm thick) prior to annealing. The silicon nitride layer was very effective in preventing the transportation of gold during annealing.

Metallographic and SEM examination of the (C)/Ta/Au samples that were capped with silicon nitride and annealed revealed that the metallized regions had a microstructure of equi-axed grains with well-defined grain boundaries and a mosaic substructure, which typifies an annealed metallic microstructure. The electrical response of the sample which was capped during annealing was essentially the same as the sample which had not been capped. Recapping and further annealing of the sample for an additional hour at 885°C produced no significant change in the electrical response of the sample. Consequently, one may postulate that the reaction of the thin film of tantalum with the diamond substrate had been completed within the first hour of anneal and that the reaction products remained stable during the subsequent hour of anneal.

A tantalum film, approximately 8 nm thick, was simultaneously deposited on a face of each of two diamond samples. One of the samples was retained in the as-deposited condition, while the other sample was capped and annealed for 1 h at 885°C. Secondary ion mass spectrometry (SIMS) was used to analyze the as-deposited sample and the annealed sample, after removing the silicon nitride cap. SIMS results indicated that shallow penetration of tantalum into the diamond substrate may have occurred during annealing.

A diamond sample that had been metallized with a 12-nm thick titanium film, overlaid by a 170-μm-thick gold film, and capped and annealed for 1 h at 775°C (to prevent the high-temperature allotropic transformation) exhibited an electrical response similar to that obtained with (C)/Ta/Au samples. An additional hour of annealing at the same temperature did not significantly change the electrical response of the (C)/Ti/Au sample.

III. Conclusions

This study demonstrates that carbide forming metal films, such as tantalum and titanium, will produce satisfactory ohmic contacts to semiconducting diamond by an annealing process conducted in the solid state.

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References

DC and Microwave Characteristics of InAlAs/InGaAs Single-Quantum-Well MODFET's with GaAs Gate Barriers

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Abstract—The design and performance of In$_{0.53}$Ga$_{0.47}$As/In$_{0.53}$Al$_{0.47}$As modulation-doped field-effect transistors (MODFET's) have been optimized by incorporating a single In$_{0.53}$Ga$_{0.47}$As quantum-well channel and a thin strained GaAs gate barrier layer. These help to lower the output conductance and gate leakage current of the device, respectively. The dc performance of 1-μm gate devices is characterized by extrinsic transconductances of 320 mS/mm at 300 K and 450 mS/mm at 77 K and a best value of $f_T = 35$ GHz is derived from S-parameter measurements. This value of the cutoff frequency is the best reported for a 1-μm gate device with this material system.

The ternary semiconductor In$_{0.53}$Ga$_{0.47}$As has demonstrated its potential for high-speed device applications and for optoelectronic integration in the 1.3–1.7-μm wavelength range where optical fibers have minimum loss and dispersion. A high low-field electron mobility, high electron velocity, and large Γ–L separation are some of the favorable material properties. Formation of a 2-DEG in In$_{0.53}$Al$_{0.47}$As/In$_{0.53}$Ga$_{0.47}$As modulation-doped heterostructures leads to further improvement in the carrier transport properties. Impressive device performance has been demonstrated in the field-effect transistors (FET’s) made with this heterostructure system [1]–[3]. However, InAlAs/InGaAs modulation-doped FET’s (MODFET’s) usually have two shortcomings: a) very high gate leakage current and low drain breakdown, possibly due to significant alloy clustering in heavily doped InAlAs [4]; and b) high output conductance as well as poor pinch-off characteristics mainly due to the high background conductivity ($\sim 0.5–1.0 \times 10^{16}$ cm$^{-2}$) in the undoped InGaAs buffer layer. It was shown recently that an undoped InAlAs layer underneath the gate is very effective in reducing the gate leakage [5]. In this letter we report the result of dc and microwave measurements on 1.0-μm gate devices in which features have been incorporated to circumvent the problems mentioned above. These are a quantum-well channel and a thin GaAs layer beneath the gate contact. It has been reported that carrier confinement in the quantum well leads to smaller short-channel effects [6] and smaller energy loss of carriers under high-field conditions [7]. A high ratio of transconductance $g_m$ to output conductance $g_o$ for a high dc voltage gain is, therefore, expected.

A schematic diagram of the device structure is shown in Fig. 1. Four different samples having different top layers as shown in Table I were used for the investigation of Schottky contact properties. All the structures were grown lattice-matched to (100) Fe-doped SI InP substrate by molecular beam epitaxy (MBE). A growth temperature of 490°C and a growth rate of 1.1 μm/h were maintained during the entire growth. The thickness and doping level of the doped InAlAs layer were decided from calculation of the threshold voltage using a charge control model [8], [9].

Devices were made by standard photolithography and lift-off techniques. Ohmic contacts were formed after isolation mesas were defined, followed by gate formation with Ti(500 Å)/Au(3000 Å). Low-resistance source and drain ohmic contacts were made by electron-beam evaporating a layered metallization consisting of Ni(50 Å)/Ge(500 Å)/Au(1200 Å)/Ni(100 Å)/Ti(500 Å)/Au(1000 Å) and alloying them in an AG Associates' halogen lamp annealing station under flowing N$_2$. A two-step anneal cycle was used [10] with an anneal at 300°C for 10 s followed by a second anneal at 400°C for 10 s. A contact resistance of 0.2 Ω-mm was measured by the TLM method.

The $I$–$V$ characteristics of Schottky diodes between gate and source were measured on 20 × 100-μm gate FET structures. Reverse leakage currents of Schottky diodes formed on four different top layers are listed in Table I. It is clear that the leakage currents are very small and comparable with doped (3 × 10$^{17}$ cm$^{-2}$) GaAs and undoped InAlAs top layers. However, the current is large with doped (3 × 10$^{17}$ cm$^{-2}$) InAlAs and (AlAs)$_n/(InAs)_2$ monolayer superlattice top layers. Furthermore, the GaAs top layer is quite effective in reducing the gate leakage current even though its thickness (100 Å) is much larger than the critical thickness (∼30 Å) with 3.7 percent lattice mismatch [11]. When undoped InAlAs is used underneath the gate, a highly doped InGaAs needs to be grown on the top of this layer to reduce the source resistance between gate and source. Therefore, a precise control of the gate recess is required so that the gate can be formed on the thin undoped InAlAs. This step can be avoided if the gate metals are deposited directly on the GaAs top layer since the doping in this layer is good enough for ohmic contact formation. The reason for a high leakage current in sample D is not clear and...
the only reason that can be offered at this time is that the growth of monolayer superlattices by the MBE system needs further study.

Next 1-μm gate FET's were fabricated with sample C as well as with sample E, which has a device structure similar to that of C but has a 0.5-μm InGaAs buffer instead of the quantum well. Drain current–voltage characteristics of $1 \times 75$-μm gate FET's measured at 300 K in samples C and E are shown in Fig. 2(a) and (b), respectively. It is to be noticed that the output conductance is reduced markedly in sample C compared with that in sample E. The transconductance-to-output conductance ratio of 100 in sample C is estimated at $V_{gs} = -1.0$ V from Fig. 2(a). The maximum extrinsic transconductances in sample C varied from 280 to 320 mS/mm. The 77 K drain current–voltage characteristics in this device are shown in Fig. 2(c). As expected, the maximum transconductance increases up to 450 mS/mm and the pinch-off characteristic is also improved.

The microwave $S$-parameters were measured at 300 K in the range of 1.1–18.1 GHz using a Cascade probe and an HP 8510 network analyzer under various bias conditions. Fig. 3 shows $S$ parameters of a typical 1-μm gate FET in sample C measured at $V_{gs} = 0$ V and $V_{ds} = 3.0$ V and modeled results. From the equivalent circuit data cutoff frequency $f_{t}$ as large as 35 GHz is calculated. A maximum available power gain of 13 dB at 10 GHz is achieved. The power gain is expected to be improved by reducing the thickness of the undoped InAlAs
spacer and increasing the doping level of the doped InAlAs layer.

In conclusion, we have demonstrated improved device performance of a quantum-well InAlAs/InGaAs MODFET. It was found that doped GaAs is effective in reducing the gate leakage current. A very high $g_m/g_d$ ratio was achieved and the value of $f_T = 35$ GHz calculated is the best so far in a 1-$\mu$m gate device with this heterostructure material system.

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REFERENCES


[3] K. S. Seo and P. Bhattacharya, "Studies on an In$_{0.52}$Ga$_{0.48}$As/In$_{0.52}$


